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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,599	02/11/2004	Ching-Wu Tseng	JCLA12098	4941

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

GM

Office Action Summary	Application No.	Applicant(s)	
	10/777,599	TSENG ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: GNDA (e.g. see page 11, paragraph 0035: lines 15 and 17) is not shown in any figure. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are also objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: VA', 131, and VOUT1 of Fig. 1 are not identified within the description. . Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet

should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 11, paragraph 0035, lines 14-18 need clarification. For example, does the "output stage" refer to "131" shown in Fig. 1, and do the "low level GNDA" (line 15) and the "high level VDDA" (line 18) both refer to output "VOUT1" of the same figure? Page 12, line 12 "VOUT1B" should be --VOUT2B-- to correspond to what is shown in Fig. 2, and also described on line 15 of page 12. Paragraph 0041 on page 13 is confusing and needs clarification because it appears PMOS 301 is turned on when the clock TTL voltage signal remains high. Therefore, it is suggested "is turned" on line 1 of the paragraph be changed to --turns--, and on line 2 of the same paragraph, add --and-- after "level," to help clarify the paragraph's first sentence. Also in paragraph 0041, "PMOS" on line 3 should be --NMOS--, and "are turn off" on line 4 should be either --turn off-- or --are turned off-- to improve word flow. Since lines 3-4 of paragraph 0044 (on page 15) indicate the pulses VA and VB are provided when voltage signal VIN changes state, it is not understood why there are extra VA and VB pulses when VIN remains stable (e.g. high or low). For example, in each of Figs. 6-9, although VIN is shown changing state only three times, each figure shows five pulses for at least pulse VA. Therefore, what causes those extra two pulses? It is believed "FIG. 3" on page

15, line 15 was meant to be --FIG. 9-- since that figure does show the currents being described. Appropriate corrections are required.

Claim Objections

Claims 14-18 are objected to because of the following informalities: Claim 14, line 9 "the first" should be --a first--, and line 13 "a first" should be --the first-- to ensure the identifying labels of the "first control signal" are in the proper sequence (e.g. to provide an antecedent basis). It is suggested "the other" on line 15 of claim 14 be changed to --another-- or --a second-- to minimize the possibility that "the other terminal" phrase can imply that this terminal has already been cited within the claim. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. Claim 1, lines 8-9 are misleading with respect to the gate of the second transistor being connected to the first control signal. For example, this limitation implies the second transistor's gate actually receives the same control signal that is processed by the AND gate (e.g. see lines 2). However, aren't these signals different from one another (e.g. see VA' and VA in the applicants' own Fig. 2), and therefore would not be considered the same signal? Related to this problem, does "the first control signal" on line 2 of claim 4 refer to the signal connected to the second transistor's gate, or the signal received and processed by the AND gate? It is not clear how the third-fifth transistors of claim 6 actually relate to the AND gate, and the

transistor device with first-second transistors, already recited within claim 1. For example, if the AND gate and first/second transistors of claim 1 are replaced by the third-fifth transistors of claim 6, how can the limitations of claim 1 now be valid, or does claim 6 still allow the first transistor to receive the synchronizing signal produced by the AND gate, and the second transistor's gate to be connected to the first control signal, as recited within claim 1? It is not understood what "the capacitor comprises a parasitic capacitor for a transistor" means in claim 8. For example, does this refer to the parasitic capacitance of either the first or second transistor, to the capacitance of another (but unidentified) transistor, or is the capacitor a discrete device (e.g. another transistor actually configured as a capacitor)? Claim 9, line 2 "a sixth transistor" implies third-fifth transistors that have not been identified within the claim's chain of dependency. If the AND gate processes, and the second transistor receives, the "first control signal", as recited within claim 1, how can the "first control signal" be both low and high voltage signals as recited within claim 12? For example, are these signals complementary to one another, and thus they will share a common phase (e.g. transition as the same time), wherein one will be at a high level while the other is at a low level? Claim 14, lines 5-6 "both electrically connected to a ground" is confusing. For example, can the second and third transistors share a common terminal (e.g. they're connected in parallel) which is electrically connected to ground? It is not understood in claim 14 how the first/second transistors' connection to a first contact point relates to the drain of the second transistor being connected to the switch. For example, it appears the drain/switch connection corresponds to the first contact point, but if that is the case, why aren't these relationships clarified better? Similar to claim 8 described above, it is not understood what "the capacitor comprises a parasitic capacitor for a transistor" means in claim 15. For example, does

this refer to the parasitic capacitance of any of the first-third transistors, or to the capacitance of another transistor (e.g. configured as a capacitive device)?

Claims 10 and 17 each recite the limitation "the second control signal" in line 2. There is insufficient antecedent basis for this limitation in either claim.

Claim 13 recites the limitation "the third, fourth, fifth" transistors in lines 1-2 with insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitation "the switch" in line 11. There is insufficient antecedent basis for this limitation in the claim. For example, does this refer to the claimed "switch device" (recited within line 2), or a switch that might be within the device? Note: Each of lines 13-15 in claim 14 also recite "the switch."

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

In so far as being understood, claims 1-3, 7-8, and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirasawa. Fig. 26 of Hirasawa shows a voltage level shifter comprising AND gate 40 for processing first control signal ø' and input signal VI to produce synchronizing signal (ø'·VI); transistor device 6,2 with first/second transistors 6/2, with the drains of 6 and 2 connected at node 5, the source of first transistor 6 connected to ground 9, the source of second transistor 2 connected to voltage source E2, the gate of 6 connected to

synchronizing signal (ø'·VI), and the gate of 2 connected to control signal ø (which has a higher voltage than, but still at the same phase of, the first control signal ø'); and capacitor 7 connected between first contact point 5 (i.e. the drains of 6 and 2) and ground, wherein capacitor 7 will store a signal level of the first contact point. Although Fig. 26 does not show a buffer with its input coupled to first contact point 5, Hirasawa discloses, and/or shows, examples that can use an output supplied through an inverter (e.g. see column 6, lines 53-57; column 7, lines 25-27; and inverter 30 of Figs. 7, 16, and 24). Therefore, it is understood that output 0_1 (first contact point 5) of Fig. 26 can be provided to the input of a buffer (e.g. CMOS inverter 30) to provide an inverted output (with respect to output 0_1) if required, anticipating claim 1. Since first/second transistors 6/2 are NMOS/PMOS transistors, claims 2 and 3 are anticipated, respectively. Using inverter 30 shown in Hirasawa's Figs. 7, 16, and 24 as an example of a buffer that can be connected to first contact point 5 of Fig. 26, the buffer comprises PMOS/NMOS transistors 31/32, respectively and claim 7 is anticipated. One of ordinary skill in the art would understand that the effective capacitance of capacitor 7 will also be at least somewhat associated with the parasitic capacitances of the MOS transistors within the transistor device, and the buffer. Therefore, claim 8 is anticipated. Fig. 27 shows first control signal ø' and input signal VI are both low voltage signals (e.g. ranging between 0V and E_1V), wherein signal ø and voltage source E_2 are understood to range between 0V and the higher voltage E_2V. Therefore, AND gate 40 can be considered as comprising a low voltage transistor device (e.g. some type of transistor device operating on voltages up to E_1V), and transistor device 6/2, buffer 30, and capacitor 7 can be considered as comprising high voltage transistor devices (e.g. operating on voltages up to E_2V), anticipating claim 11. Since first control signal ø' input to AND gate 40 is a low voltage signal

(i.e. ranging between 0V and E_1V), and control signal ø is a high voltage signal (i.e. ranging between 0V and E_2V) having the same phase as first control signal ø' (e.g. see Fig. 27), claim 12 is also anticipated.

No claim is allowable as presently written.

Allowable Subject Matter

Claim 14 would be allowable if rewritten or amended to satisfactorily overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. There is presently no strong motivation to modify or combine any prior art reference to ensure the voltage level shifter comprises the switch device, controlled by the first control signal connected to the gates of the first/second transistors, wherein the switch is connected between the first contact point and the second contact point as recited within claim 14.

Claims 4-5, and 15-18 would be allowable if rewritten to satisfactorily overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference to ensure the voltage shifter also comprises a switch, controlled by the first control signal (e.g. that is also connected to the gate of the second transistor as shown in the applicants' own Fig. 2), wherein the switch is coupled between the first contact point and the first transistor's drain, as recited within claim 4 (upon which claim 5 depends). Dependent claims 15-18 depend on independent claim 14, described above with respect to its allowable material (e.g. the switch is connected between the first and second contact points).

Note: No allowable determination is being presently made with respect to claims 6, 9-10, and 13. The relationships between all the claimed transistors, and/or the first/second control signals, must be satisfactorily clarified before the claims can be considered as reciting allowable material.

Prior Art

The prior art references cited on the accompanying PTO-892 are deemed relevant to at least some of the claimed limitations. Although Fig. 1(d) of On shows an input transistor device with first-third transistors 26,30,31, and inverter 28,29, that correspond to the input transistor device and buffer of the applicants' Fig. 3 (e.g. see input transistor device 301,313,311 and buffer 331), and recited within claim 14. However, the On reference lacks the switch that is connected between the first and second contact points, wherein that switch is controlled by the same first control signal that is connected to the gates of the first/second transistors within the input transistor device. Fig. 3B of Lines shows a voltage level shifter comprising an input transistor device comprising three transistors; buffer 284-288, and transistor 290 controlled by output WL of the buffer, and connected between voltage source Vpp and the buffer's input. Although this reference also lacks the switch connected between the first/second contact points (i.e. understood to correspond to the output of the input transistor device, and the input of the buffer), these references should be reviewed and considered.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

14 June 2005

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